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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,484	09/28/2001	Toru Ishida	H-1013	2783

7590 10/20/2004

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,484	ISHIDA ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/964484 Attorney's Docket #: H-1013
Filing Date: 9/28/01;

Applicant: Ishida et al.

Examiner: Alexander Williams

Applicant's Response, filed 7/14/04, has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 5 and 7 to 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishizawa et al. (U.S. Patent # 6,5735,671 B1).

Claim 1 and similar claims 5, 11, 18, 19, 23, 24, 28 and 29, Nishizawa et al. **(figures 1 to 27)** specifically **figures 12 and 13** show a semiconductor device **1** comprising: a first semiconductor chip **34a** having on one main surface thereof a control circuit, a first bonding pad **R/B**, and a plurality of second bonding pads **/WE**; a second semiconductor chip **34b** having on one main surface thereof a memory circuit and a third bonding pad **R/B** and disposed on the one main surface of the first semiconductor chip, the memory circuit being controlled in accordance with a control signal generated in the control circuit on the first semiconductor chip; a first lead **39A** having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of second leads **39a** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a first bonding wire **43a** for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead; a plurality of second bonding wires **43a** for connecting the plural second bonding pads on the first semiconductor chip with the inner lead portions of the plural second leads; a third bonding wire **43b** for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead; and a resin seal member **55** for sealing the first and second semiconductor chips, the first, second and third bonding wires, and the inner lead portions of the first and second leads. In claim 1 and similar claims 5, 11, 18, 19, 23, 24, 28 and 29, Nishizawa et al. show wherein the control signal generated in the control circuit is outputted from the first bonding pad on the first semiconductor chip and is inputted to the third bonding pad on the semiconductor chip through the first bonding wire, the first lead and the third bonding wire.

2. A semiconductor device according to claim 1, Nishizawa et al.'s second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

3. A semiconductor device according to claim 1, Nishizawa et al. show an another main surface opposed of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.

4. A semiconductor device according to claim 1, Nishizawa et al.'s first and third bonding wires are connected to one and same surface of the first lead.
7. A semiconductor device according to claim 5, Nishizawa et al.'s plural bonding pads on the first semiconductor chip include a first bonding pad, wherein the plural bonding pads on the second semiconductor chip include a second bonding pad, wherein the first bonding pad is electrically connected to an inner lead portion of one of the plural leads through a first bonding wire, wherein the second bonding pad is electrically connected to an inner lead portion of one of the plural leads through a second bonding wire, and wherein the serial data are outputted from the first bonding pad and inputted to the second bonding pad through the first bonding wire, one of the plural leads, and the second bonding wire.
8. A semiconductor device according to claim 5, Nishizawa et al.'s second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.
9. A semiconductor device according to claim 5, Nishizawa et al. show wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.
10. A semiconductor device according to claim 6, Nishizawa et al. show wherein the first and second bonding wires are connected to one and same surface of one of the plural leads.
12. A semiconductor device according to claim 11, Nishizawa et al. show wherein the second semiconductor chip is formed in a quadrangular shape in plan, and wherein the plural third bonding pads are arranged along at least one side of the second semiconductor chip.
13. A semiconductor device according to claim 11, Nishizawa et al. show wherein the second semiconductor chip is formed in a quadrangular shape in plan, and wherein the plural third bonding pads are arranged along at least two sides contiguous to each other of the second semiconductor chip.
14. A semiconductor device according to claim 11, Nishizawa et al. show wherein the first bonding pad and the plural third bonding pads are bonding pads for signal.
15. A semiconductor device according to claim 11, Nishizawa et al. show wherein the second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

16. A semiconductor device according to claim 11, Nishizawa et al. show wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.
17. A semiconductor device according to claim 11, Nishizawa et al. show wherein the first and third bonding wires are connected to one and same surface of the first lead.
20. A semiconductor device according to claim 19, Nishizawa et al. show wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the first semiconductor chip and a second center line orthogonal to the first center line, and wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the second semiconductor chip and a second center line orthogonal to the first center line.
22. A semiconductor device according to claim 21, Nishizawa et al. show wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the first semiconductor chip and a second center line orthogonal to the first center line, and wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the second semiconductor chip and a second center line orthogonal to the first center line.
25. A semiconductor device according to claim 24, Nishizawa et al. show wherein the second semiconductor chip is bonded to the first main surface of the first semiconductor chip through an adhesive layer.
26. A semiconductor device according to claim 25, Nishizawa et al. show wherein the adhesive layer is formed by a bonding resin film.
27. A semiconductor device according to claim 25, Nishizawa et al. show wherein the distance from the first main surface of the first semiconductor chip to the second main surface of the second semiconductor chip is smaller than the thickness of the first semiconductor chip.
30. A semiconductor device according to claim 29, Nishizawa et al. show wherein the bonding pads on the second semiconductor chip are larger in plane size than the bonding pads on the first semiconductor chip.
31. A semiconductor device according to claim 29, Nishizawa et al. show wherein the second bonding wires each have a first portion extending in a direction perpendicular to

the first main surface of the second semiconductor chip and a second portion extending along the first main surface of the second semiconductor chip, and wherein the first portion is positioned above the inner lead portions.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (U.S. Patent # 6,573,5671 B1) in view of Ohie (U.S. Patent # 6,580,164 B1).

Nishizawa et al. show the features of the claimed invention as detailed above, but fail to explicitly show first semiconductor chip is a chip for a microcomputer, and wherein the second semiconductor chip is a chip for an EEPROM.

Ohie is cited for showing a first semiconductor chip is a chip for a microcomputer, and wherein the second semiconductor chip is a chip for an EEPROM for the purpose of making it possible to develop and debug software.

Therefore, it would be obvious to one of ordinary skill in the art to use Ohie's EEPROM as a semiconductor chip to modify Nishizawa et al.'s semiconductor chip for the purpose of making it possible to develop and debug software.

The listed references are cited as of interest to this application, but not applied at this time.

Response

Applicant's arguments filed 7/14/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

Field of Search	Date
U.S. Class and subclass: 257/723-25,728,777,784,786,666,676,685,686,692, 696,698,796,777,684	11/25/02 7/10/03 3/4/04 10/15/04
Other Documentation: foreign patents and literature in 257/723- 25,728,777,784,786,666,676,685,686,692, 696,698,796,777,684	11/25/02 7/10/03 3/4/04 10/15/04
Electronic data base(s): U.S. Patents EAST	11/25/02 7/10/03 3/4/04 10/15/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
10/15/04

Alexander Williams
Primary Examiner